ONR Final Report
Reliable Advanced Electronic Systems Research
July 1, 1988- June 30, 1991

Contract number: N00014-85-K-0600

Project Summary

The SDI Mission requires the production of systems that can operate reliably for long time periods without maintenance. Such systems are feasible only if they can be manufactured and assembled without defects, and run-time errors can be promptly and accurately identified.

The major objectives of this project were (1) new production test methods to eliminate chips with "latent" failures; and (2) fault-tolerance structures designed specifically for temporary as well as permanent failures.

Pseudo-exhaustive test. We have shown that to realize generally accepted quality levels (10-100 DPM) for integrated circuits, it is necessary to have a test technique that will detect at least 99.99% of all possible defects. Such a technique is not feasible by extending current methods that rely on the single-stuck fault model.

The only hope for a sufficiently thorough test technique is some methodology that does not rely on the enumeration of all possible defects and which can detect performance as well as functional faults. In other words, it must be possible to use what we are calling "weak fault models," which are very general fault classes such as all faults that don't introduce state (combinational faults) or all faults that increase supply current, etc. We have developed a design method to ensure that bridging faults in an implementation do not invalidate an exhaustive test due to an increase in state. A supply current monitoring methodology for testing ECL circuits has also been developed.

Our earlier work on bridging faults has now been extended with a technique for detecting delay faults without having to enumerate the faults or network paths.

Another research thrust was the development of a pseudo-exhaustive test methodology that is both thorough and cost-effective. We have written a program to segment arbitrary combinational logic into sufficiently small segments where exhaustive test of each segment is possible. The pseudo-exhaustive test approach is very different from the traditional techniques of either ignoring non single-stuck faults or trying to enumerate and generate tests for other fault models. Since there are too many faults to completely enumerate, such approaches cannot guarantee sufficiently high fault coverage. The risk involved in pursuing pseudo-exhaustive test is that it will not be possible to develop a completely general methodology, but this risk is justified due to the importance of the objective.

Run-time error detection. Run-time error detection is necessary to avoid false actions and to permit the elimination of failed modules. Traditional techniques for detecting run-time errors rely on duplicate subsystems or on the use of embedded checkers and error-detecting codes. Duplication is very expensive not only in terms of cost but also weight. Code methods are effective only for defects that correspond to errors within the capability of the codes used, and require substantial hardware overhead. We have developed a methodology that uses coprocessors called watchdog processors to implement run-time error detection. The watchdog systems are much smaller than duplicate systems and are more general than any of the coding based systems.

Latent failures are initially undetected failures that cause errors after the system is in operation. We have studied the effects on system operation of know failure mechanisms such as oxide breakdown and demonstrated that delay and pattern sensitive faults are important failure modes. Techniques are being developed that will detect these faults.

June 23, 1993

We have also demonstrated that the effect of these defects (gate oxide shorts) on system operation depends on voltage and temperature. They can thus cause intermittent faults. We are developing techniques to permit detection of such defects. Designs for error detectors that function correctly in the presence of non-classical faults are being developed.

High-level design for test. To ensure the correctness of a design, the most promising approach is to start with a VERY high level specification and then to automate the design process. In particular, the resulting design should not only meet performance specifications correctly, but should also guarantee good testability at reasonable cost. We are developing a design system that will accept VHDL design specifications and automatically generate a testable implementation. The ingredients in this design system include testable implementations and test protocols for standard macrofunctions such as multiplexers, shifters, comparators, and adders. Self-testing implementations are of particular interest. We have developed a technique for allocating registers to enable effective and cost-efficient BILBO testing. A new BIST structure, called *Orthogonal BIST*, that reduces BIST overhead has been developed.

The only demonstrated solution for on-chip or on-board test response evaluation uses a Linear Feedback Shift Register to compact the test response. The major problem with this technique is the difficulty in determining whether faulty chips will pass the test because of "aliasing" in the signature register and of choosing design parameters to constrain the aliasing to an acceptably low value. While it is possible to simulate the test with the signature register in place, this process is too costly for realistic designs — every fault considered (usually single-stuck faults) must be simulated for all test inputs (fault dropping to reduce simulation cost is not possible when the signature register is included in the simulation). It is also possible to use a probabilistic model to estimate the probability of aliasing, but for typical values of test length and size of the signature register the evaluation of the model is computationally prohibitively expensive. Thus, the only hope is to develop useful bounds on the alias probability. We have developed bounds that permit the alias probability to be estimated very simply as a function of test length and signature register size. Thus, a specification of allowed alias probability can be met by choosing these two parameters according to the bound. Earlier bounds by Ivanov and Williams do not facilitate such a design technique.

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To Whom it may Concern:

Enclosed is a copy of Prof. Edward J. McCluskey's final report for ONR Contract number: N00014-85-K-0600, Reliable Advanced Electronic Systems Research.

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Sincerely,

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encls.

PUBLICATIONS LIST

JOURNAL PAPERS

[Lau 89] Lau, C., C.M. Hu, and E.J. McCluskey, "Research in Advanced Electronic System Reliability," *Naval Research Reviews,* Vol. XLI, pp. 9-19, Three/1989.

[McCluskey 89] McCluskey, E.J., and F. Buelow, "IC Quality and Test Transparency," *IEEE Trans. on Industrial Electronics,* Vol. 36, No. 2, pp. 197-202, May 1989.

[McCluskey 90] McCluskey, E.J., "Design Techniques for Testable Embedded Error Checkers," *Special Issue on Fault-Tolerant Systems, Computer,* pp. 84-88, July 1990.

[Mourad 89] Mourad, S., and E.J. McCluskey, "Testability of Parity Checkers," *IEEE Trans. on Industrial Electronics,* Vol. 36, No. 2, pp. 254-262, May 1989.

[Saxena 90] Saxena, N.R., and E.J. McCluskey, "Control-Flow Checking Using Watchdog Assists and Extended-Precision Checksums," *IEEE Trans. Comput.,* Vol. 39, No. 4, pp. 554-559, April 1990.

[Saxena 90] Saxena, N.R., and E.J. McCluskey, "Analysis of Checksums, Extended-Precision Checksums and Cyclic Redundancy Checks," *IEEE Trans. Comput.,* Vol. 39, No. 7, pp. 969-975, July 1990.

[Saxena 92] Saxena, N.R., P. Franco, and E.J. McCluskey, "Simple Bounds on Signature Analysis Aliasing for Random Testing," Special Issue on Fault-Tolerant Computing, *IEEE Trans. Comput.*, pp. 638-645, May 1992.

CONFERENCE PAPERS

[Avra 90] Avra, L., and E.J. McCluskey, "Behavioral Synthesis of Testable Systems with VHDL," *COMPCON Spring '90,* San Francisco, CA, pp. 410-415, Feb. 26 - Mar. 2, 1990. (CRC TR 89-10)

[Avra 92] Avra, L., "Orthogonal Built-In Self-Test," *COMPCON Spring 92*, San Francisco, CA, pp. 452-457, Feb. 24-28, 1992.

[Makar 89] Makar, S., and E.J. McCluskey, "The Critical Path for Multiple Faults," *1989 IEEE Int. Conf. on Computer-Aided Design,* Santa Clara, CA, pp. 162-165, Nov. 6-9, 1989. (CRC TR 89-3)

[McCluskey 90] McCluskey, E.J., "Design for Test Overview," *Microelectronic System Education Conference & Exposition*, San Jose, CA , July 29 - Aug. 1, 1990.

[McCluskey 91] McCluskey, E.J., "Who Needs Design for Testability?," *Dig. 1991 IEEE Int. Solid-State Circuits Conf.*, San Francisco, Feb. 13-15, 1991.

[Millman 88] Millman, S.D., and E.J. McCluskey, "Detecting Bridging Faults with Stuck-at Test Sets," Proc. 1988 Int. Test Conf., Washington, DC, Sep. 12-14, 1988.

[Millman 89] Millman, S., and E.J. McCluskey, "Detecting Stuck-Open Faults with Stuck-At Test Sets," *IEEE Custom Integrated Circuits Conference,* San Diego, CA, May 15-18, 1989.

[Millman 90] Millman, S.D., E.J. McCluskey, and J.M. Acken, "Diagnosing CMOS Bridging Faults with Stuck-At Fault Dictionaries," *Proc. 1990 Int. Test Conf.*, Washington, DC, pp. 860-870, Sep. 10-12, 1990.

[Nanya 88] Nanya, T., S. Mourad, and E.J. McCluskey, "Multiple Stuck-at Fault Testability of Self-Testing Checkers," *Dig. 18th Annu. Int. Symp. Fault-Tolerant Comput.* (FTCS 18), Tokyo, Japan, June 27-30, 1988.

[Norman 90] Norman, R.H., and E.J. McCluskey, "Design for Integrity," *Advanced Microelectronics Technology Qualification, Reliability and Logistics Workshop*, San Diego, CA, Aug. 28-30, 1990.

[Saxena 89] Saxena, N., and E.J. McCluskey, "Control-Flow Checking Using Watchdog Assists and Extended-Precision Checksums," *Dig. 19 th Annu. Int. Symp. Fault-Tolerant Comput. (FTCS-19),* Chicago, IL, June 21-23, 1989.

[Saxena 89] Saxena, N., and E.J. McCluskey, "Arithmetic and Galois Checksums," *1989 IEEE Int. Conf. on Computer-Aided Design*, Santa Clara, CA, pp. 570-573, Nov. 6-9, 1989. (CRC TR 89-3)

[Saxena 90] Saxena, N.R., and E.J. McCluskey, "Bounds on Aliasing Probabilities under Bernoulli Error Model for Signature Analysis," *Proc. 1990 Int. Test Conf., Poster Session*, Washington, DC, Sep. 10-12, 1990.

[Udell 88] Udell, J.G. Jr., and E.J. McCluskey, "Partial Hardware Partitioning: A New Pseudo-Exhaustive Test Implementation," *Proc. 1988 Int. Test Conf.*, Washington, DC, Sep. 12-14, 1988.

[Udell 89] Udell, J., and E.J. McCluskey, "Pseudoexhaustive Test and Segmentation; Formal Definitions and Extended Fault Coverage Results," *Dig. 19th Annu. Int. Symp. Fault-Tolerant Comput. (FTCS 19)*, Chicago, IL, June 21-23, 1989.

[Wang 89] Wang, L.T., M. Marhoefer, and E.J. McCluskey, "A Self-Test and Self-Diagnosis Architecture for Boards Using Boundary Scans," *European Test Conference*, Paris, France, pp. 119-126, Apr. 12-14, 1989.

TECHNICAL REPORTS

(CRC TR 88-7) Udell, J.G. Jr., and E.J. McCluskey, "Partial Hardware Partitioning: A New Pseudo-Exhaustive Test Implementation," Sep. 1988.

(CRC TR 88-8) Amer, H.A., and E.J. McCluskey, "Safe and Unsafe faults in CMOS Exclusive-Or Gates with Gate Oxide Shorts," Sep. 1988.

(CRC TR 88-10) Udell, J.G. Jr., and E.J. McCluskey, "Circuit Reduction for Efficient Segmentation," Dec. 1988.

(CRC TR 88-11) Udell, J.G. Jr. , and E.J. McCluskey, "An Efficient Segmentation Program for Pseudo-Exhaustive Test," Dec. 1988.

(CRC TR 88-12) Udell, J.G. Jr., and E.J. McCluskey, "Pseudo-Exhaustive Test and Segmentation: Formal Definitions and Extended Fault Coverage Results," Dec. 1988.

(CRC TR 89-1) Udell, J.G. Jr., "Pseudo-Exhaustive Testing of Digital Integrated Circuits," Apr. 1989.

(CRC TR 89-4) Hao, H., and E.J. McCluskey, "Survey of Combinational Shifter Implementations," Oct. 1989.

(CRC TR 89-5) Millman, S.D., and E.J. McCluskey, "Detecting Stuck-Open Faults with Stuck-At Test Sets," Dec. 89.

(CRC TR 89-6) Millman, S.D., and E.J. McCluskey, "Bridging, Transition, and Stuck-Open Faults in Self-Testing CMOS Checkers," Dec. 89.

(CRC TR 89-7) Millman, S.D., and E.J. McCluskey, "Pseudorandom Test for Bridging Faults," Dec. 89.

(CRC TR 89-8) Millman, S.D., J.M. Acken, and E.J. McCluskey, "Diagnosing CMOS Bridging Faults with Stuck-At Fault Dictionaries," Dec. 89.

(CRC TR 89-9) Millman, S., "Nonclassical Faults in CMOS Digital Integrated Circuits," Dec. 89.

(CRC TR 90-1) Yamamura, H. and E.J. McCluskey, "Fault Analysis of ECL Gates with Device Defects using SPICE," Mar. 1990.

(CRC TR 90-2) Avra, L., and E.J. McCluskey, "On the Behavioral Synthesis of Testable Systems with VHDL," May 1990.

(CRC TR 90-3) Makar, S.R., and E.J. McCluskey, "Minimal Single Stuck-at Tests For Multiplexers," June 1990.

(Numerical Analysis Project, Manuscript NA-89-12) Boley, D., G.H. Golub, S. Makar, N. Saxena, and E.J. McCluskey, "Backward Error Assertions for Checking Solutions to Systems of Linear Equations," Nov. 1989.

(CRC TR 90-5) Fukazawa, T., and E.J. McCluskey, "Assertions for Dynamic Error Detection on a Parallel Processor," Nov. 1990.

(CRC TR 90-6) Yamamura, H., "A Scheme to Detect Non-Functional Faults in ECL Circuits," Nov. 1990.
(CRC TR 90-7) Makar, S.R., and E.J. McCluskey, "Implementing Fault Models in Verilog," Nov. 1990.
(CRC TR 90-9) Avra, L., "Allocation and Assignment in High-Level Synthesis for Self-Testable Data Paths," Dec. 1990.
(CRC TR 90-10) Yamauchi, H., "Mixed Level and High Level ATPG," December 1990.
(CRC TR 90-11) Saxena, N.R., E.J. McCluskey, and P. Franco, "Bounds on Signature Analysis Aliasing for Random Testing," Dec. 1990.
(CRC TR 91-1) Hao, H., and E.J. McCluskey, "Resistive Shorts Within CMOS Gates," Feb. 1991.
(CRC TR 91-2) Saxena, N.R., E.J. McCluskey, and P. Franco, "Refined Bounds on Signature Analysis Aliasing for Random Testing," Feb. 1991.
(CRC TR 91-3) Saxena, N.R., E.J. McCluskey, and S. Makar, "Linear Complexity Assertions for Sorting Algorithms," Feb. 1991.
(CRC TR 92-2) "Preprint of a paper from the 1992 International Test Conference," Baltimore, MD, Sep. 20-24, 1992.
Ma, S., and E.J. McCluskey, "Non-Conventional Faults in BiCMOS Digital Circuits."
(CRC TR 92-3) Touba, N., "Reducing Synchronization in Concurrent Behavioral Descriptions, Aug. 1992.

BOOK CONTRIBUTIONS

[McCluskey 90] McCluskey, E.J.,"Foreword" in *Structured Logic Testing*, Prentice-Hall Inc., Englewood Cliffs, NJ, 1990.
[McCluskey 90] McCluskey, E.J., "Half a century of Logic Synthesis," in *Logic and Architecture Synthesis*, pp. 3-8, P. Michel and G. Saucier, ed. *North-Holland, 1991* (CRC TR 90-4)